DOCKET T9625.00

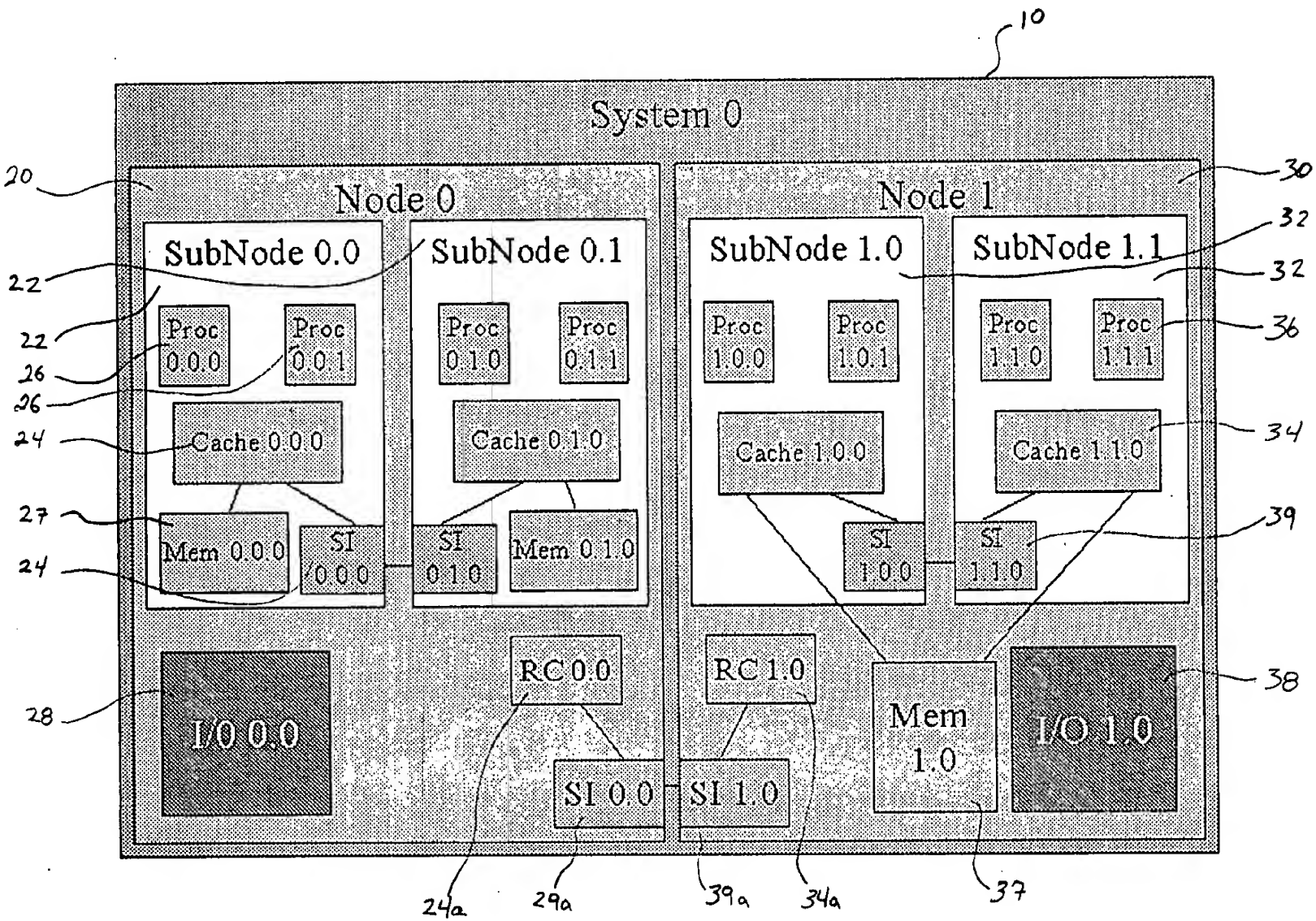


FIG. 1

FIG. 2

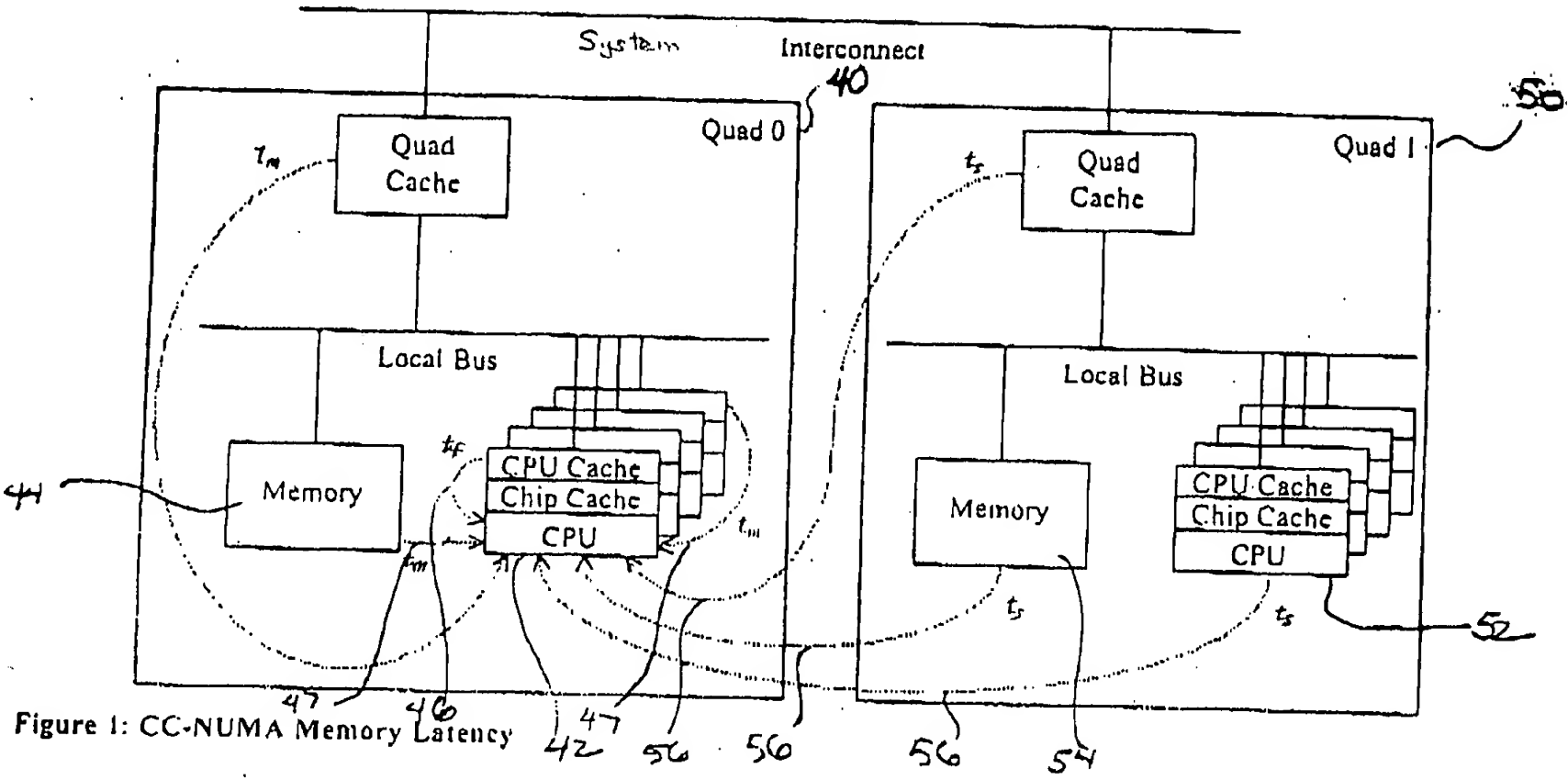


Figure 1: CC-NUMA Memory Latency

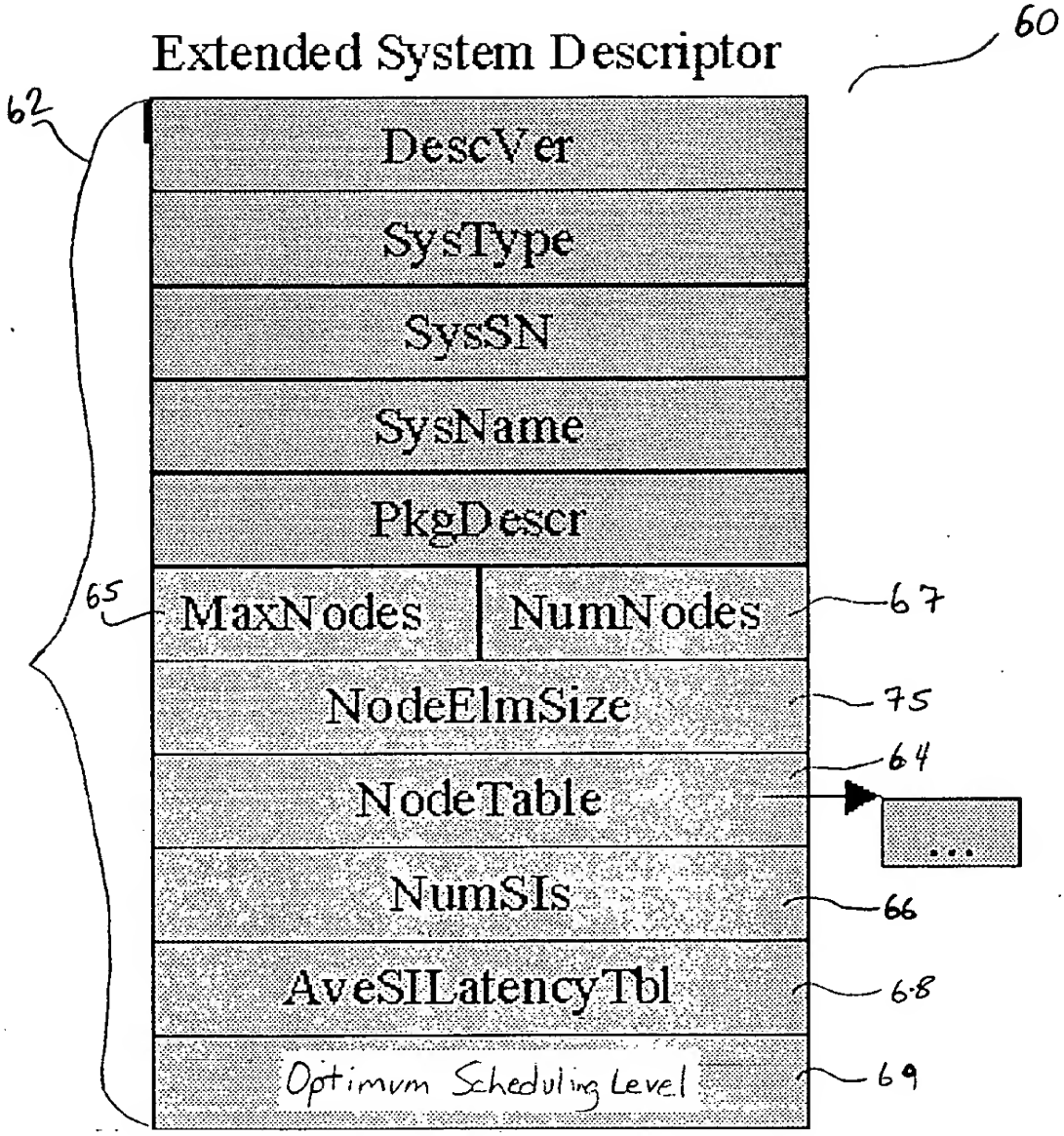
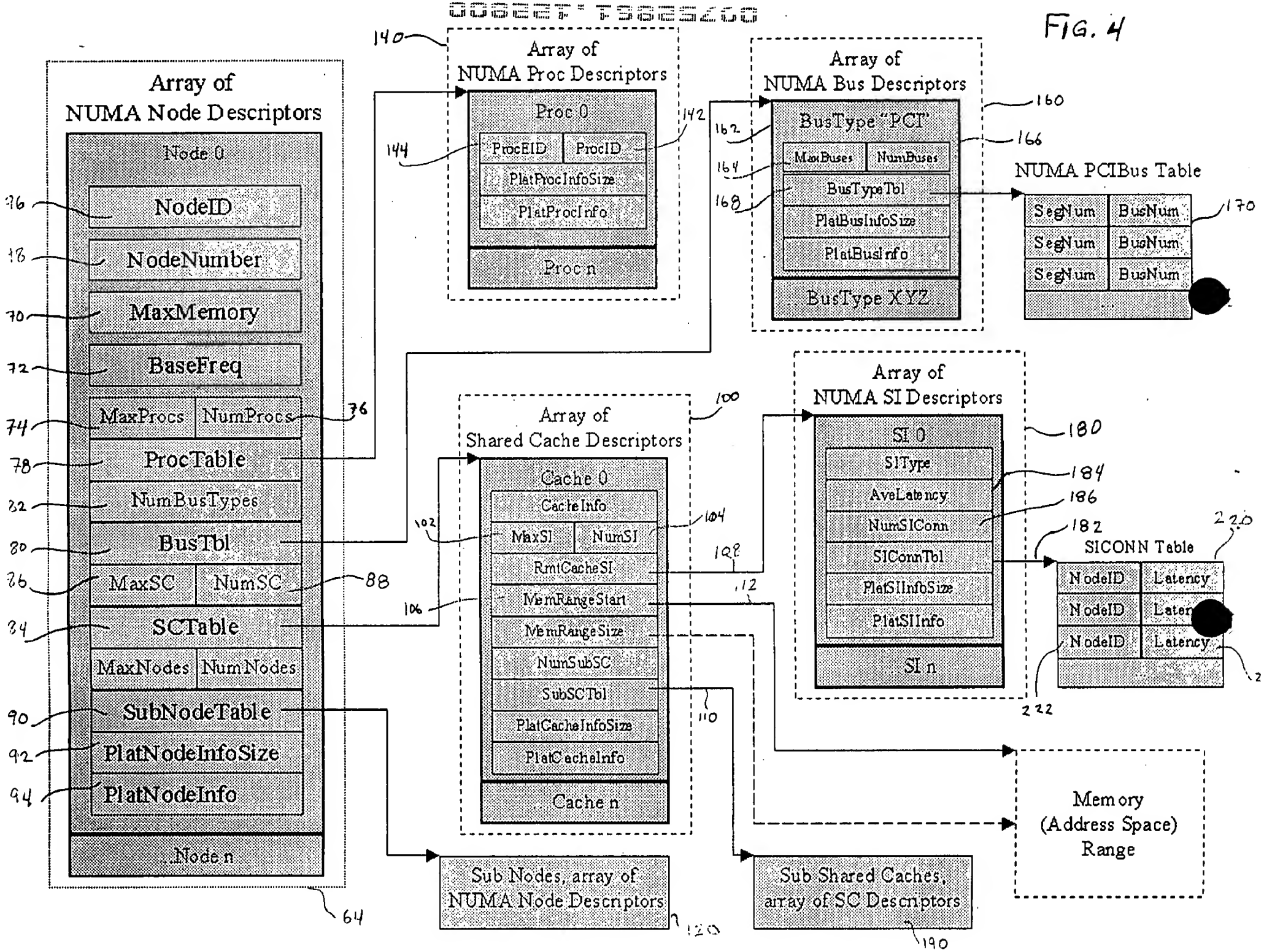

Extended System Descriptor
60
62
DescVer
SysType
SysSN
SysName
PkgDescr
65
MaxNodes
NumNodes
67
NodeElmSize
75
64
NodeTable
...
NumSIs
66
AveSILatencyTbl
68
Optimum Scheduling Level
69

FIG. 3

FIG. 4


Array of
NUMA Node Descriptors
Node 0
NodeID
NodeNumber
MaxMemory
BaseFreq
MaxProcs
NumProcs
ProcTable
NumBusTypes
BusTbl
MaxSC
NumSC
SCTable
MaxNodes
NumNodes
SubNodeTable
PlatNodeInfoSize
PlatNodeInfo
Node n
64
Array of
NUMA Proc Descriptors
140
Proc 0
ProcEID
ProcID
142
144
PlatProcInfoSize
PlatProcInfo
Proc n
Array of
NUMA Bus Descriptors
160
BusType "PCI"
162
MaxBuses
NumBuses
166
164
BusTypeTbl
168
PlatBusInfoSize
PlatBusInfo
BusType XYZ
NUMA PCIBus Table
SegNum
BusNum
170
Array of
Shared Cache Descriptors
100
Cache 0
CacheInfo
MaxSI
NumSI
102
104
RmtCacheSI
108
MemRangeStart
112
MemRangeSize
NumSubSC
SubSCTbl
110
PlatCacheInfoSize
PlatCacheInfo
Cache n
Array of
NUMA SI Descriptors
180
SI 0
SIType
184
AveLatency
186
NumSIConn
182
SIConnTbl
PlatSIInfoSize
PlatSIInfo
SI n
220
SICONN Table
NodeID
Latency
222
Memory
(Address Space)
Range
Sub Nodes, array of
NUMA Node Descriptors
120
Sub Shared Caches,
array of SC Descriptors
190
76
74
78
82
80
86
88
84
90
92
94
96
98
106

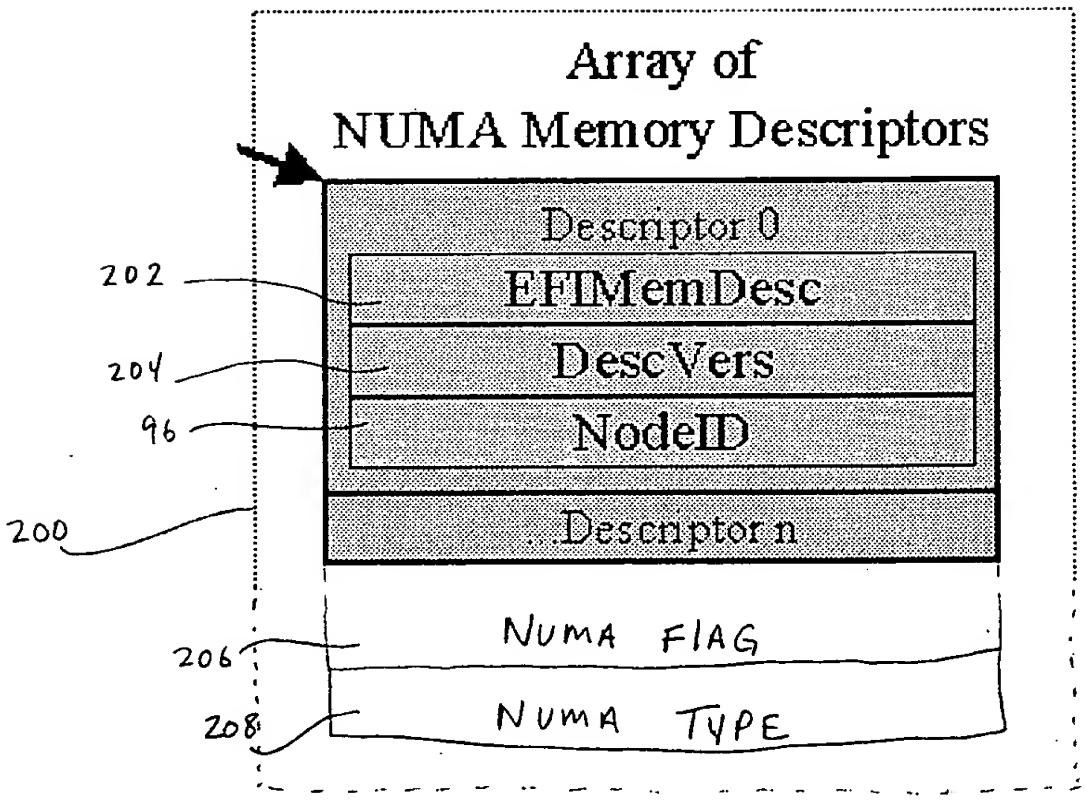
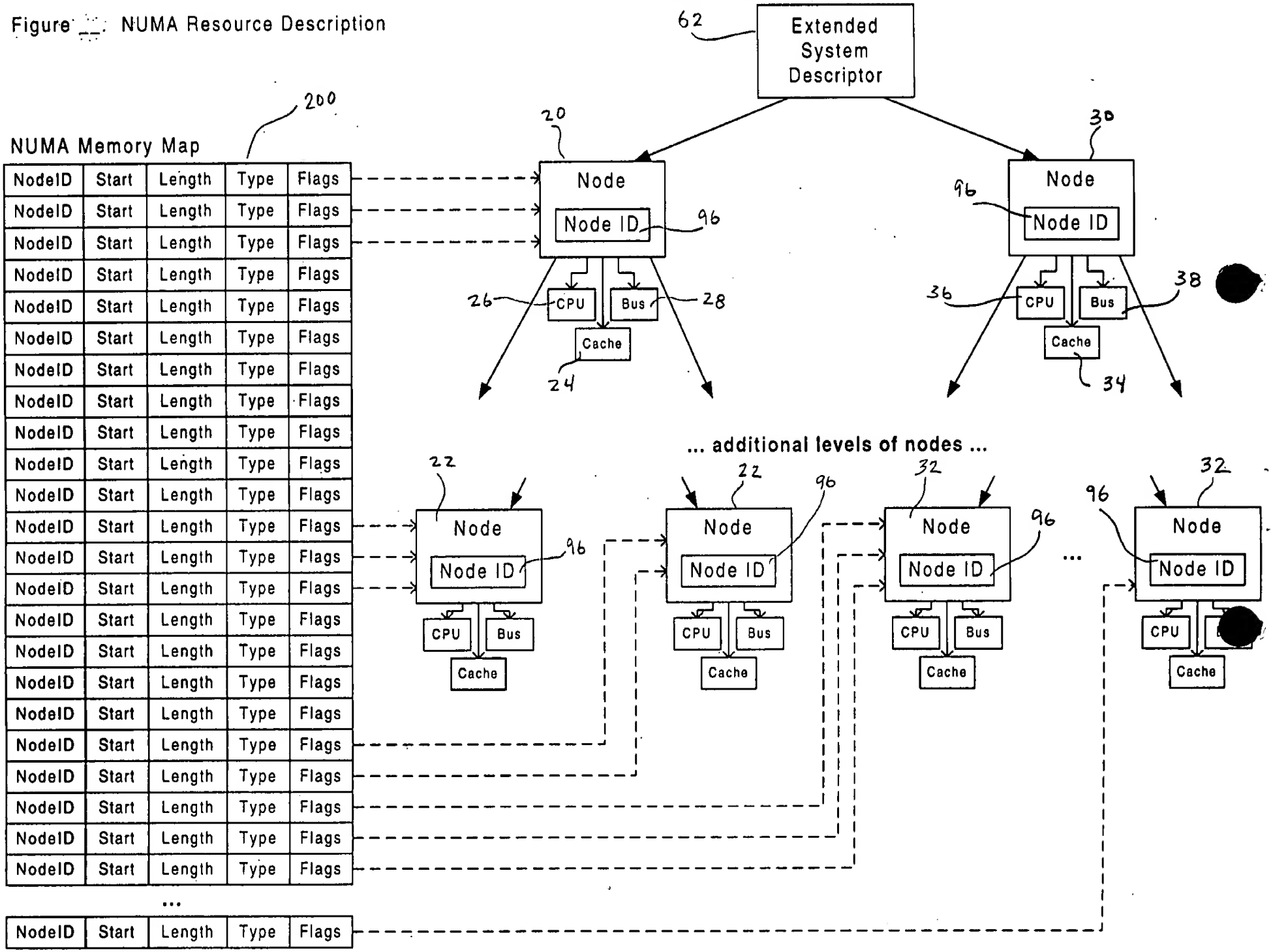

Array of
NUMA Memory Descriptors
Descriptor 0
EFIMemDesc
DescVers
NodeID
Descriptor n
NUMA FLAG
NUMA TYPE
202
204
96
200
206
208

FIG. 5

FIG. 6

Figure __: NUMA Resource Description



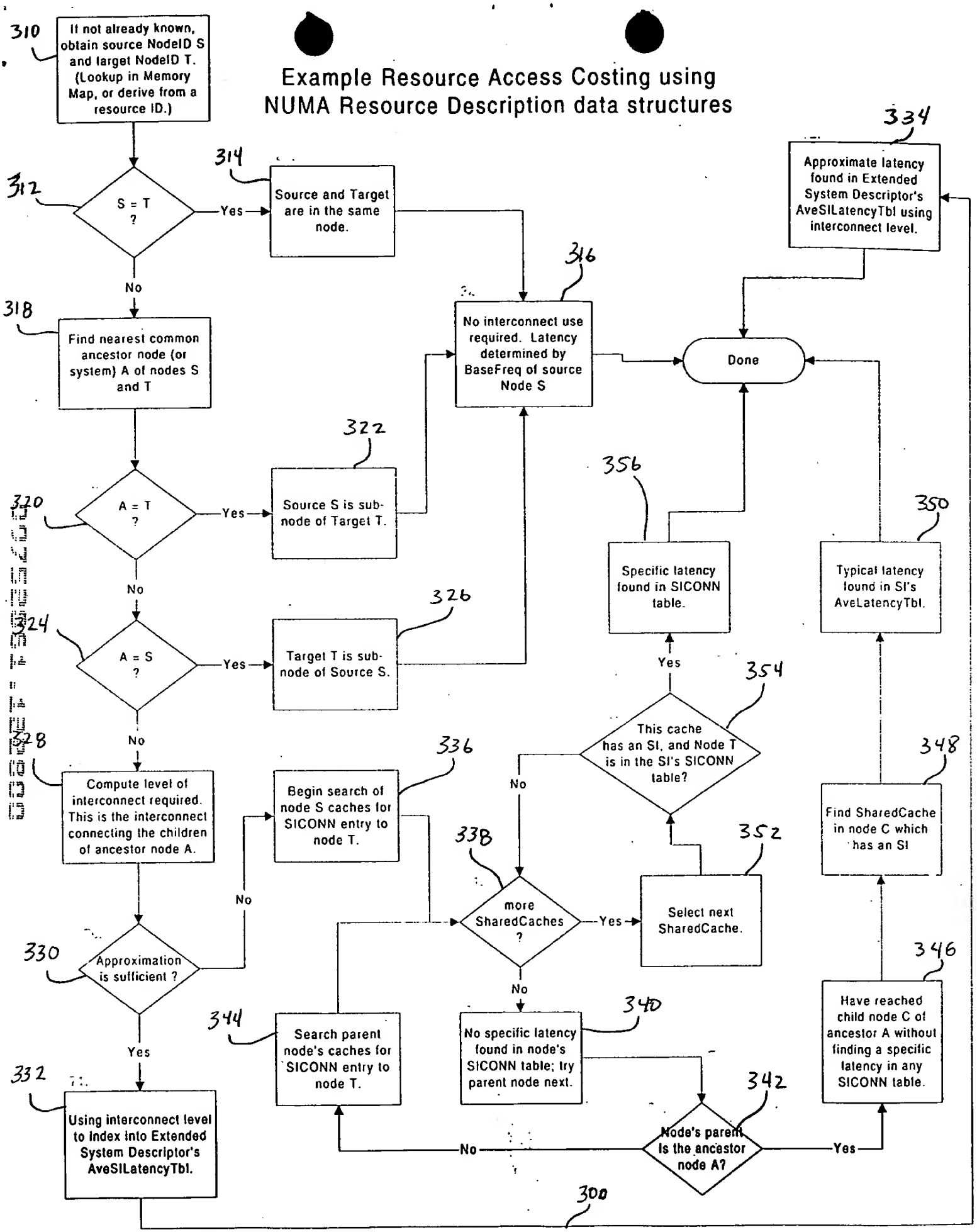

Example Resource Access Costing using NUMA Resource Description data structures
310
If not already known, obtain source NodeID S and target NodeID T. (Lookup in Memory Map, or derive from a resource ID.)
312
S = T ?
Yes
314
Source and Target are in the same node.
No
316
No interconnect use required. Latency determined by BaseFreq of source Node S
318
Find nearest common ancestor node (or system) A of nodes S and T
320
A = T ?
Yes
322
Source S is sub-node of Target T.
No
324
A = S ?
Yes
326
Target T is sub-node of Source S.
No
328
Compute level of interconnect required. This is the interconnect connecting the children of ancestor node A.
330
Approximation is sufficient ?
No
336
Begin search of node S caches for SICONN entry to node T.
Yes
332
Using interconnect level to index into Extended System Descriptor's AveSILatencyTbl.
334
Approximate latency found in Extended System Descriptor's AveSILatencyTbl using interconnect level.
Done
356
Specific latency found in SICONN table.
Yes
354
This cache has an SI, and Node T is in the SI's SICONN table?
No
338
more SharedCaches ?
Yes
352
Select next SharedCache.
No
340
No specific latency found in node's SICONN table; try parent node next.
344
Search parent node's caches for SICONN entry to node T.
342
Node's parent is the ancestor node A?
No
Yes
350
Typical latency found in SI's AveLatencyTbl.
348
Find SharedCache in node C which has an SI
346
Have reached child node C of ancestor A without finding a specific latency in any SICONN table.
300

FIG. 7